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ISL9110AIITAZ-EVAL1Z/ISL9110AIITNZ-EVAL1Z Evaluation Board User Guide

Evaluation Board Features

- ISL9110A high efficiency buck-boost regulator
- Input voltage rating from 1.8V to 5.5V
- Resistor programmable output voltage on the ISL9110AIITAZ-EVAL1Z evaluation board
- Fixed 3.3V output voltage on the ISL9110AIITNZ-EVAL1Z evaluation board
- Up to 1200mA output current
- 2.5MHz switching frequency
- Jumper selectable EN (enabled/disabled)
- Jumper selectable MODE (auto-PFM/forced-PWM)
- LED indicators for PG and BAT status outputs
- Connectors, testpoints, and jumpers for easy evaluation

Required Equipment

- Power supply capable of delivering up to 5.5V and 3A
- Electronic load
- Multimeter to measure voltages and currents
- Oscilloscope

Testpoints, Connectors, and Jumpers

TABLE 1. DESCRIPTION OF TEST POINTS

TEST POINT(S)	DESCRIPTION
TP1	VOUT Kelvin connection for efficiency measurements
TP2	LX1 (Input side of power inductor)
TP3	PGND (Power ground)
TP4	LX2 (Output side of power inductor)
TP5	PVIN Kelvin connection for efficiency measurements
TP7	PG (Open drain status output)
TP8	$\overline{BAT}$ (Open drain status output)
TP9	EN (Enable input, drive high to enable device)
TP10	MODE/SYNC (Mode input, drive low for forced PWM, or apply external clock between 2.75MHz and 3.25MHz for external sync)
TP11, TP13, TP14	GND (Ground)

TABLE 2. DESCRIPTION OF CONNECTORS

CONNECTOR	DESCRIPTION
J1	Header for connecting input power
J2	Header for connecting external load

TABLE 3. DESCRIPTION OF JUMPERS

JUMPER	DESCRIPTION
J3	Jumper to select EN input logic state. Set EN = VIN to enable device, or set EN = GND to disable device.
J4	Jumper to select MODE input logic state. Set MODE = VIN to enable auto-PFM mode, or set MODE = GND to select forced PWM mode. To use external sync feature, remove this jumper and apply an external clock between 2.75MHz and 3.25MHz on the MODE testpoint (TP10) or center pin on the J10 header.
J5	Jumper to enable PG LED. Remove this jumper when measuring quiescent current.
J6	Jumper to enable $\overline{BAT}$ LED. Remove this jumper when measuring quiescent current.

Quick Setup Guide

1. Install jumpers on J5 and J6 to enable the status LEDs.
2. Install jumper on J3, shorting EN to VIN.
3. Install jumper on J4, shorting MODE to VIN.
4. Connect power supply to J1, with voltage setting between 1.8V and 5.5V.
5. Connect electronic load to J2.
6. Place scope probes on VOUT testpoint, and other testpoints of interest.
7. Turn on the power supply.
8. Monitor the output voltage startup sequence on the scope. The waveforms will look similar to that shown in Figure 1 and Figure 2.
9. Turn on the electronic load.
10. Measure the output voltage with the voltmeter. The voltage should regulate within data sheet spec limits.
11. To determine efficiency, first remove jumpers J5 and J6 to eliminate LED currents. Then measure input and output voltages at the Kelvin testpoints TP5 and TP1 and measure the input and output currents. Calculate efficiency based on these measurements.
12. To test external sync, remove the jumper at J4, then apply an external clock between 2.75MHz and 3.25MHz on the MODE input (testpoint TP10, or the center pin of header J4).

Typical Start-up Waveforms

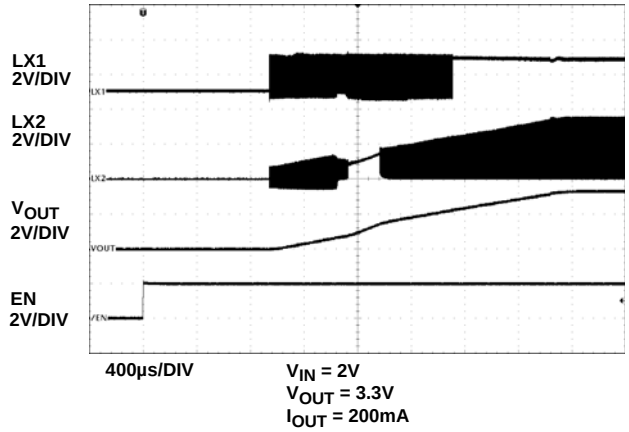

FIGURE 1. ISL9110A START-UP WITH V_{IN} = 2V and V_{OUT} = 3.3V

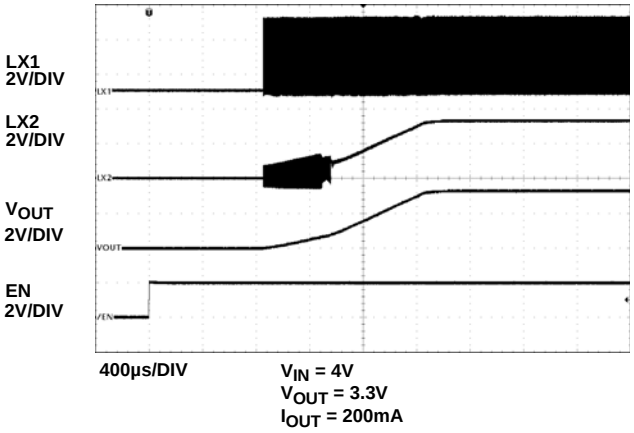

FIGURE 2. ISL9110A START-UP WITH V_{IN} = 4V and V_{OUT} = 3.3V

Output Voltage Programming

The ISL9110AIITAZ-EVAL1Z evaluation board uses resistors to program the output voltage. To change the output voltage, resistor R2 should be removed and replaced with a resistor value corresponding to the desired output voltage, as shown in Table 4. A precision resistor with 1% tolerance should be used.

TABLE 4. OUTPUT VOLTAGE PROGRAMMING

DESIRED OUTPUT VOLTAGE (V)	R2 RESISTOR VALUE (kΩ)
2.0	665
2.5	470
3.0	365
3.3	324
3.4	309
4.0	249
4.5	215
5.0	191

ISL9110AIITAZ-EVAL1Z Evaluation Board Schematic

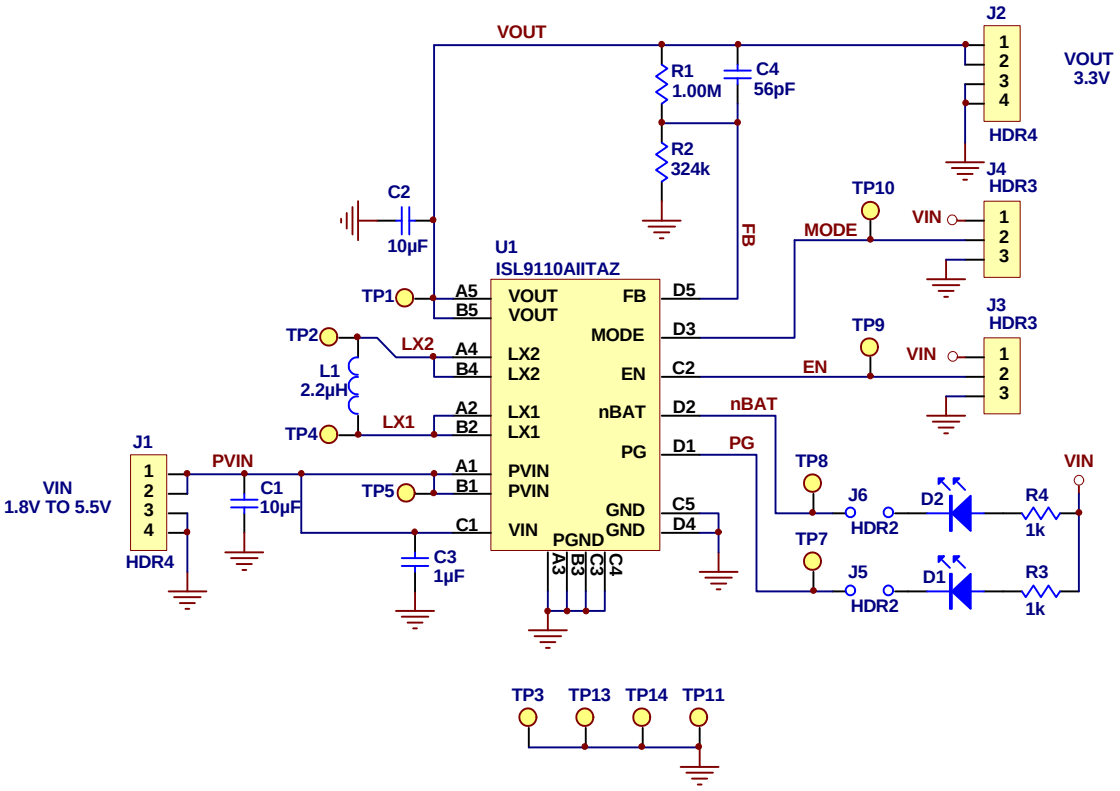

FIGURE 3. ISL9110AIITAZ-EVAL1Z EVALUATION BOARD SCHEMATIC

TABLE 5. ISL9110AIITAZ-EVAL1Z EVALUATION BOARD BILL OF MATERIALS

ITEM#	QTY	DESIGNATORS	PART TYPE	FOOTPRINT	DESCRIPTION	VENDORS
1	1	U1	ISL9110AIITAZ	W4x5.20 WLCSP	Intersil ISL9110 Buck-Boost Regulator with Adjustable Output Voltage	INTERSIL
2	1	L1	2.2µH	4x4mm	NR4018T2R2M	Taiyo Yuden
3	2	C1, C2	10µF/6.3V/X5R	0805	GRM21BR71A106KE51L	Murata
4	1	C3	1µF/6.3V/X5R	0402	Capacitor, Generic	ANY
5	1	C4	56pF	0402	Capacitor, Generic	ANY
6	1	R1	1MΩ, 1%	0402	Resistor, Generic	ANY
7	1	R2	324kΩ, 1%	0402	Resistor, Generic	ANY
8	2	R3, R4	1kΩ	0603	Resistor, Generic	ANY
9	2	D1, D2	LED, RED	1.6x0.8	LED, RED, SMD	ANY
10	2	J5, J6	HDR-2	HDR-2	Vert. Pin Header, 2-Pin, 0.1” Spacing, Generic	ANY
11	2	J3, J4	HDR-3	HDR-3	Vert. Pin Header, 3-Pin, 0.1” Spacing, Generic	ANY
12	2	J1, J2	HDR-4	HDR-4	Vert. Pin Header, 4-Pin, 0.1” Spacing, Generic	ANY
13	12	TP1, TP2, TP3, TP4, TP5, TP7, TP8, TP9, TP10, TP11, TP13, TP14	TEST POINT	TEST POINT	Test Point, Thru-Hole, White, Mouser 534-5002	KEYSTONE

ISL9110AIITNZ-EVAL1Z Evaluation Board Schematic

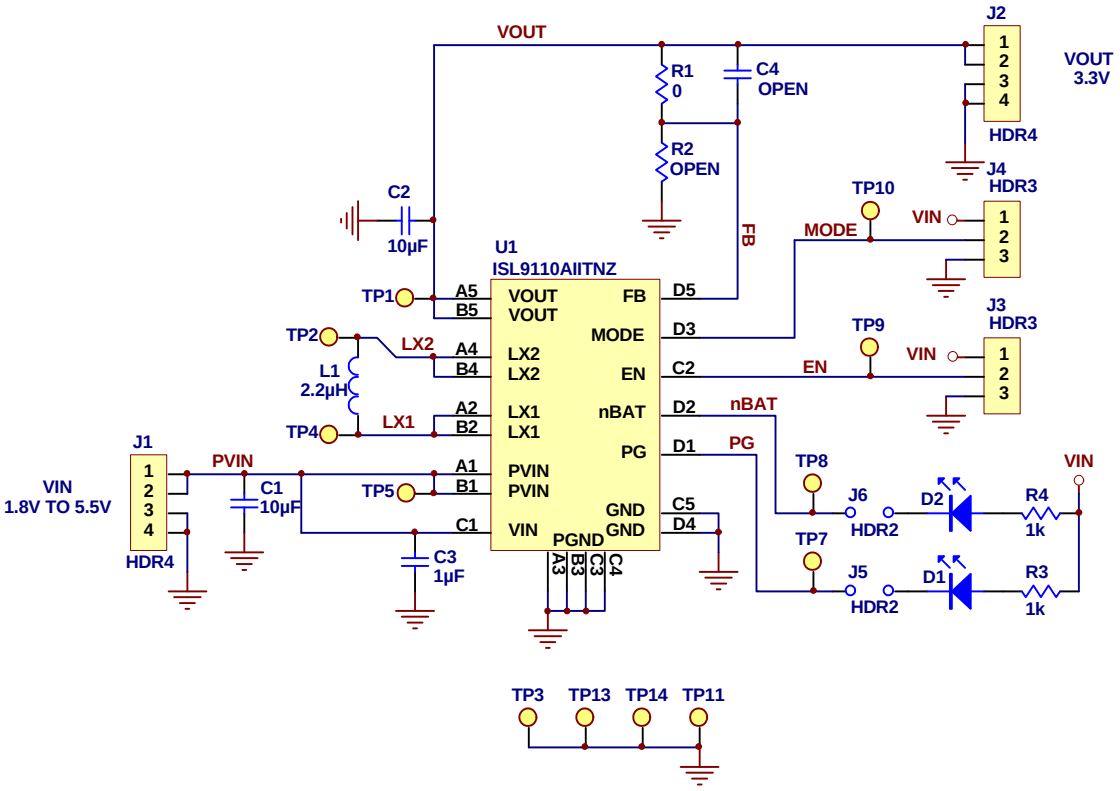

FIGURE 4. ISL9110AIITNZ-EVAL1Z EVALUATION BOARD SCHEMATIC

TABLE 6. ISL9110AIITNZ-EVAL1Z EVALUATION BOARD BILL OF MATERIALS

ITEM#	QTY	DESIGNATORS	PART TYPE	FOOTPRINT	DESCRIPTION	VENDORS
1	1	U1	ISL9110AIITNZ	W4x5.20 WLCSP	Intersil ISL9110 Buck-Boost Regulator with Fixed 3.3V Output	INTERSIL
2	1	L1	2.2µH	4x4mm	NR4018T2R2M	Taiyo Yuden
3	2	C1, C2	10µF/6.3V/X5R	0805	GRM21BR71A106KE51L	Murata
4	1	C3	1µF/6.3V/X5R	0402	Capacitor, Generic	ANY
5	1	C4	OPEN	0402	Not installed	ANY
6	1	R1	0Ω	0402	Resistor, Generic	ANY
7	1	R2	OPEN	0402	Not installed	ANY
8	2	R3, R4	1kΩ	0603	Resistor, Generic	ANY
9	2	D1, D2	LED, RED	1.6x0.8	LED, RED, SMD	ANY
10	2	J5, J6	HDR-2	HDR-2	Vert. Pin Header, 2-Pin, 0.1” Spacing, Generic	ANY
11	2	J3, J4	HDR-3	HDR-3	Vert. Pin Header, 3-Pin, 0.1” Spacing, Generic	ANY
12	2	J1, J2	HDR-4	HDR-4	Vert. Pin Header, 4-Pin, 0.1” Spacing, Generic	ANY
13	12	TP1, TP2, TP3, TP4, TP5, TP7, TP8, TP9, TP10, TP11, TP13, TP14	TEST POINT	TEST POINT	Test Point, Thru-Hole, White, Mouser 534-5002	KEYSTONE

Evaluation Board Layout

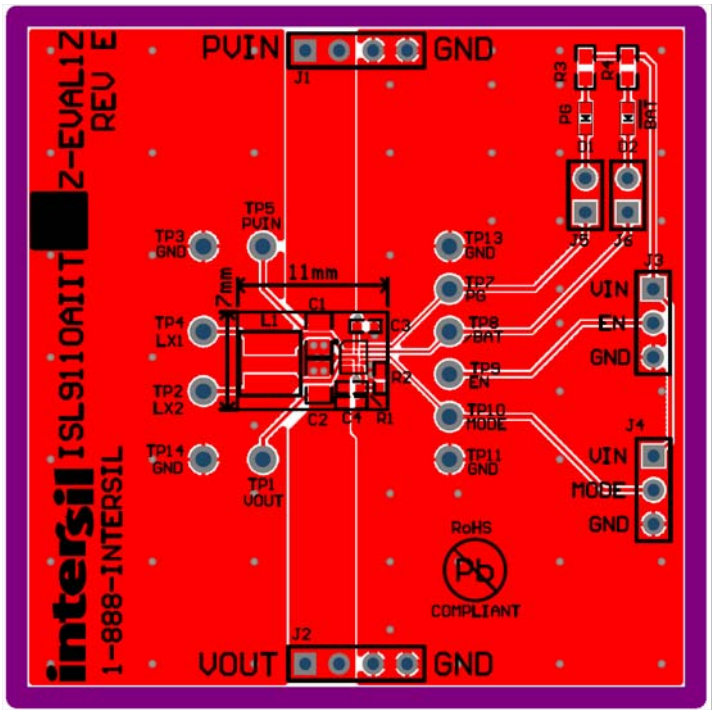

FIGURE 5. ISL9110A EVALUATION TOP SILKSCREEN

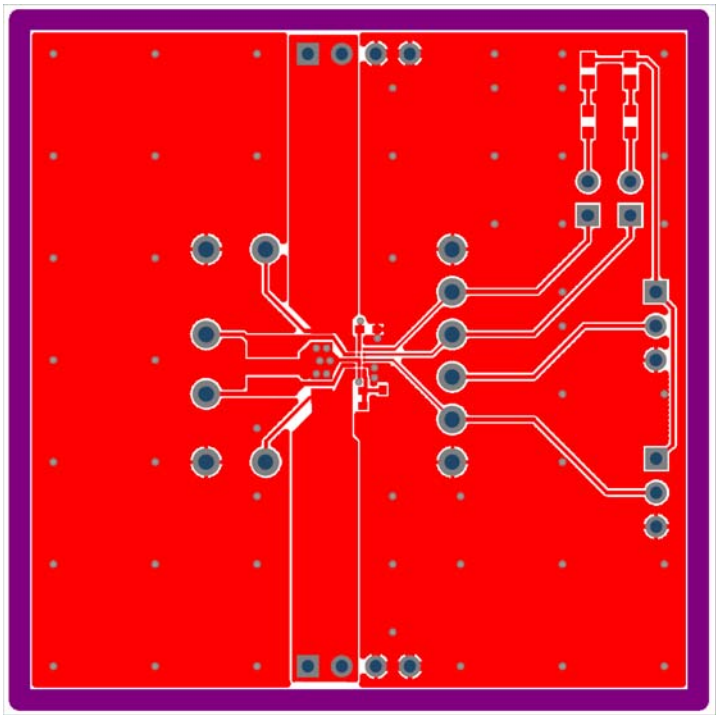

FIGURE 6. ISL9110A EVALUATION BOARD TOP COPPER

Evaluation Board Layout (Continued)

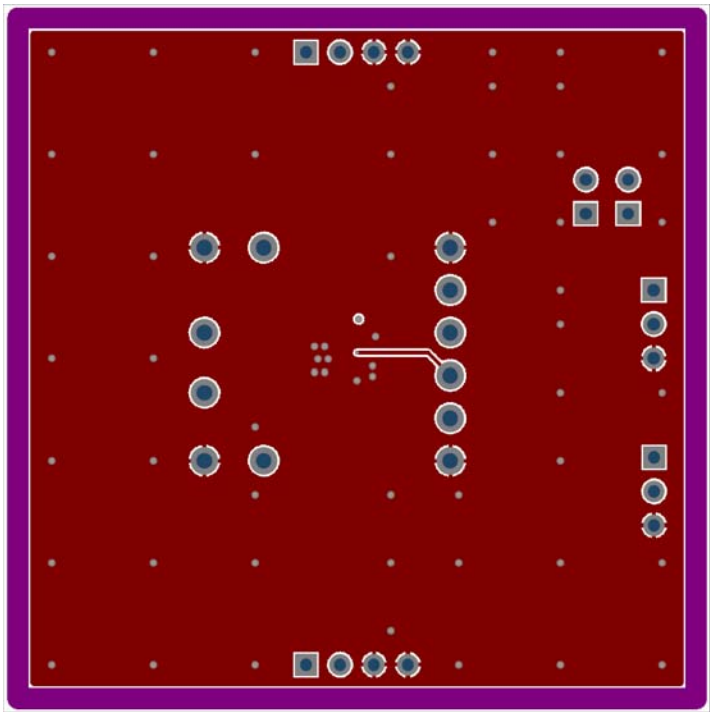

FIGURE 7. ISL9110A EVALUATION BOARD MID1 LAYER (GND)

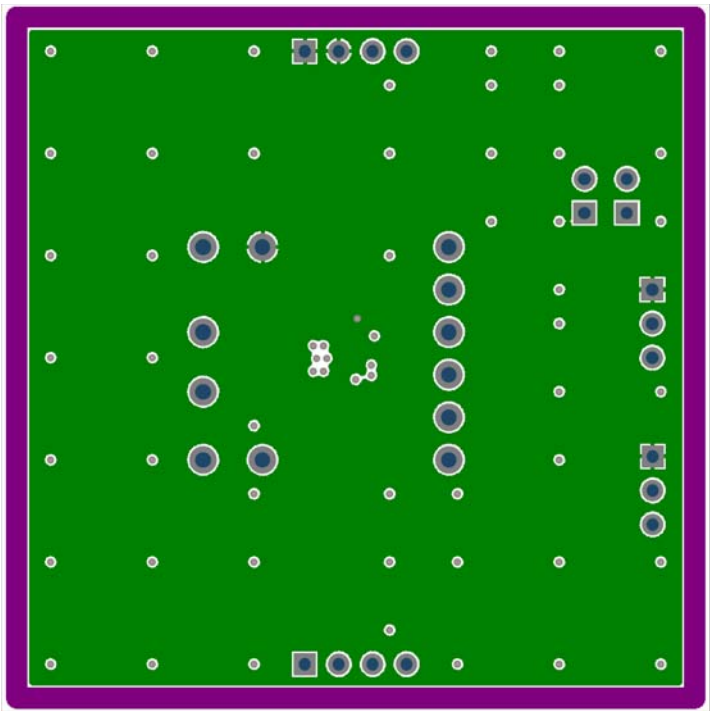

FIGURE 8. ISL9110A EVALUATION BOARD MID2 LAYER (PVIN)

Evaluation Board Layout (Continued)

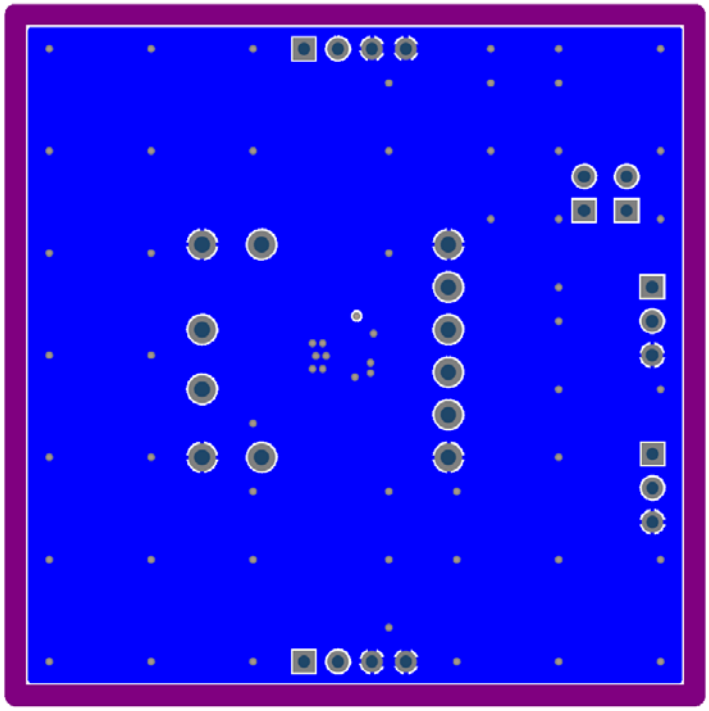

FIGURE 9. ISL9110A EVALUATION BOARD BOTTOM LAYER (GND)